REMARKS

Claim 16 has been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention. The applicants respectfully submit that no new matter has been added. It is believed that this Response is fully responsive to the Office Action dated September 13, 2002.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

Claims 1 - 11 and 16 - 19 are currently pending in this patent application. Non-elected claims 12 - 15 will be canceled, as requested by the Examiner.

Claims 17 and 19, added in the applicants' Amendment of July 5, 2002, stand rejected under 35 USC §112, first paragraph, for the specific reasons set forth in the last full paragraph on page 2 of the outstanding Action. More particularly, the Examiner has taken the position that the recitation that each of the claimed source region is "annular," as set forth in each of claims 17 and 19 is not described in the applicants' specification, as originally filed.

The applicants respectfully request reconsideration of this rejection.

In response, the applicants respectfully submit that, as clearly noted in line 10, page 14 of the applicants' original specification (and as originally shown in the applicants' Figures 1 and 2), the applicants' Figure 2 is described as a sectional view taken along the cross-sectional line A-A in the applicants' Figure 1, the applicants' Figure 1 showing six cells 3_1 through 3_6, each being in a rectangular configuration. In addition, as noted in lines 22 - 25, page 27 of the applicants' specification, as originally filed, each of the cells 3_1 through 3_6 need not be limited to a rectangular configuration, but can take the shape of "for example, circular cells." As such, the claimed source regions being annular are supported in the applicants' specification, as originally filed.

Accordingly, the withdrawal of the outstanding rejection under 35 USC §112, first paragraph, is in order, and is therefore respectfully solicited.

Claims 16 - 19 stand rejected under 35 USC §112, second paragraph, for the specific reasons set forth in the first through third full paragraphs on page 3 of the outstanding Action. The applicants respectfully request reconsideration of this rejection.

First, it is the applicants' position that independent claim 16 should include the following recitation: "and a conductive region of a second conductive type" in order to be consistent with the claimed semiconductor substrate recited in each of independent claims 1, 11 and 18.

Secondly, the applicants disagree with the Examiner's comments that independent claim 18 fails to further limit independent claim 11. Here, the applicants point out that the following structural limitations, which are absent in independent claim 11, are found in independent claim 18:

> wherein the transistor comprises a plurality of said source regions and outer periphery of each said source regions is exposed at a side of upper part of said trench.

Thus, contrary to the Examiner's position, claim 18 does in fact further limit the scope of independent claim 11.

Accordingly, the withdrawal of the outstanding indefiniteness rejection under 35 USC §112, second paragraph, is in order, and is therefore respectfully solicited.

As to the merits of this case, the Examiner now relies on a new reference (namely, Sapp, U.S. Patent No. 6,351,018) in rejecting claims 1 - 11 under 35 USC §103(a) based on Baliga (of record) in view of Sapp. The applicants respectfully request reconsideration of this rejection.

First, the Examiner specifically relies on the teachings of the secondary reference of Sapp in order to supplement the deficiencies in the teachings of the primary reference of Baliga in failing to "specifically state or describe a bottom part being in contact with an upper part of said drain layer."[1]

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[1] See, lines 3 and 4, page 5 of the outstanding Action.

More particularly, the Examiner has taken the position that:

> Sapp in fig. 2 and col. 2 lines 33-45 describes a bottom part of the insulating layer being in contact with upper part of drain region (col. 2 line 43-45) to provide isolation [trenches] that allow large anode contact area that connects to the trench MOSFET source terminal thus resulting in better devices.[2]

It is respectfully submitted, however, that in the last Amendment filed for this case, the following structural arrangements were highlighted in independent claims 1 and 11:

> a source electrode film provided in contact with said source region exposed at least on the side surface of said trench and electrically insulated from said gate electrode material.

As further argued in support of such claimed structural arrangements in each of independent claims 1 and 11, it was argued that significant structural arrangements of the applicants' power MOSFET 1 include the source electrode film 29 and the source region 27 in each cell 3 being in direct contact with each other on: (1) a top surface 51 of the semiconductor substrate 5, and (2) an inner circumferential surface 52 of the trench 18, and are electrically connected to each other. Consequently, the area of the source regions 27 exposed on the inner side surface 52 of the trench 18 can be increased; thereby, increasing the contact area between the source regions 27 and the source electrode film 29. By doing so, there is no need to increase the size of the source regions 27 along the substrate top surface 51; thereby, reducing the area occupied by the source regions, and the

[2] See, lines 5 - 8, page 5 of the outstanding Action.

size of the device.[3]

However, there is nothing in the Examiner's specific reliance on either the Baliga or Sapp reference, the above-discussed significant claimed structural arrangements, set forth in each of independent claims 1 and 11 (and in previously added independent claims 16 and 18), can be found.

Secondly, the Examiner responds to the applicants' arguments, set forth in the July 5, 2002 Amendment, in the following manner:

> [Applicants] argue that Baliga is not concerned with the increase in the contact area between a source region and a source electrode film by increasing the area of the source region exposed on the inner circumferential or side surface of the trench.
>
> It is noted that the above limitation is not recited in any of the pending claims and is therefore not given patentable weight.[4]

Emphasis added. Contrary to the Examiner's rebuttal argument, it is clear that each of independent claims 1, 11, 16 and 18 specifically recites the following limitations:

> a source electrode film provided in contact with said source region exposed at least on the side surface of said trench and electrically insulated from said gate electrode material.

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[3] As described in, for example, line 22, page 20 through line 14, page 21 of the applicants' specification, as originally filed.

[4] See, lines 15 - 19, page 6 of the outstanding Action. Also, see, lines 11 - 14, page 8 of the applicants' July 5, 2002 Amendment.

As discussed above, the paragraph bridging pages 7 and 8 of the applicants' July 5, 2002 Amendment explains that such claimed structural arrangement increases the contact area between the source regions 27 and the source electrode film 29 without increasing the size of the source regions 27 along the substrate top surface 51; thereby, reducing the area occupied by the source regions and the size of the device.

The applicants therefore respectfully submit that the claimed limitations alleged by the Examiner "not [to be] recited in any of the pending claims" are in fact set forth in each of independent claims 1, 11, 16 and 18, and the advantages or benefits derived therefrom clearly explained.

Accordingly, even if, *arguendo*, the teachings of Baliga and Sapp can be combined in the manner suggested by the Examiner, such combined teachings would still fall far short in fully meeting the applicants' claimed invention. Thus, a person of ordinary skill in the art would not have found the applicants' claimed invention obvious under 35 USC §103(a) based on Baliga and Sapp, singly or in combination.

In view of the above, the withdrawal of the outstanding obviousness rejection under 35 USC §103(a) based on Baliga in view of Sapp is in order, and is therefore respectfully solicited.

In view of the aforementioned amendments and accompanying remarks, claims, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, the applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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PATENT TRADEMARK OFFICE

Enclosures: Version with markings to show changes made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/660,439

IN THE CLAIMS:

Please amend claim 16 as follows:

16. (Amended) A transistor comprising:

a semiconductor substrate having a semiconductor layer, a drain layer of a first conductivity type and a conductive region of a second conductivity type formed by diffusing an impurity of the second conductivity type from a surface of said drain layer;

a trench provided such that it extends from a surface of said conductive region to said drain layer;

a source region of the first conductivity type provided inner surface of said conductive region and exposed on a side surface of said trench;

a gate insulating film provided on the side surface of said trench, an upper part of the gate insulating film being in contact with a lower part of said source region, a bottom part being in contact with an upper part of said drain layer, and a middle part being in contact with said conductive region;

a gate electrode material provided in contact with said gate insulating film in said trench;

a source electrode film provided in contact with said source region exposed at least on the side surface of said trench and electrically insulated from said gate electrode material,

wherein the transistor comprises a plurality of said source regions and outer periphery of each of said source regions is exposed at a side of upper part of said trench.